AMENDMENTS TO THE SPECIFICATION:

Please amend the paragraph beginning at page 15, line 4 as follows:

Fig. [[1]]2 shows a block diagram of an image processing apparatus in a first embodiment. The image processing apparatus in this embodiment is designed to support both discrete cosine transform and discrete wavelet transform using an irreversible 9/7 filter.

Please amend the paragraph beginning at page 18, line 15, as follows:

Fig [[2]]3 shows a detailed block diagram of the processing apparatus in this embodiment. The processing unit 20 includes latches 22 and 24, a flipflop FF19, a limiter 26, and a flipflop 20 in addition to the adder unit 21, the multiplier unit 23, and the adder/subtractor unit 25.

Please amend the paragraph beginning at page 23, line 14, as follows:

As shown in Fig. [[3]]4, the coefficient α depends on the kind of the transfer to be performed as described in the following. For encoding through the discrete wavelet transform using the irreversible 9/7 filter, the coefficient α is set to the aforementioned coefficient W1 in the event that the pixel of interest is positioned in the event numbered columns, while set to zero (0) in the event that the pixel of interest is positioned in the odd numbered columns. For decoding through the discrete wavelet transform using the irreversible 9/7 filter, the coefficient α is set to zero in the event that the pixel of interest is positioned in the even numbered columns, while set to W1 in the event that the pixel of interest is positioned in the odd numbered columns. For both encoding and decoding through the discrete cosine transform, the coefficient α is set to D0 in the event that the pixel of interest is positioned in the even numbered columns, while set to D5 in the event that the pixel of interest is positioned in the odd numbered columns.

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